WHAT IS CLAIMED IS:

1. A method for processing integrated circuit devices, the method comprising:

introducing a test wafer into a production run of wafers to form a run of wafers to be processed, each of the wafers being before a gate dielectric production process;

inserting the run of wafers into a process for gate dielectric production;

forming a siliconoxynitride layer to a predetermined thickness of less than 40 Angstroms at a predetermined temperature using a nitrogen bearing species and an oxygen bearing species;

removing the test wafer from the run;

forming a second oxidation overlying the siliconoxynitride layer to a second thickness, the second thickness being based substantially upon a nitrogen bearing concentration in the siliconoxynitride layer;

determining a difference value between the first predetermined thickness and the second thickness; and

correlating the difference value to one of a plurality of nitrogen concentrations to determine a nitrogen concentration in the first predetermined thickness.

2. The method of claim 1 wherein the second oxidation is a rapid thermal oxidation process using oxygen bearing species.

3. The method of claim 2 wherein the second thickness is greater than the first predetermined thickness.

4. The method of claim 1 wherein the process is an in-line process with production run.

5. The method of claim 1 wherein the second oxidation is greater than about 900 degrees C using an oxygen molecular species.

6. The method of claim 1 wherein the correlating is from a plot, the plot relating difference value to nitrogen concentrations.

7. The method of claim 1 wherein the determining is provided using at least an ellipsometer.

8. The method of claim 1 wherein the forming of siliconoxynitride comprises forming a silicon oxide layer overlying the wafers and introducing a nitrogen bearing species to form silicon oxynitride.

9. The method of claim 1 wherein the forming of silicon nitride layer comprises at least implanting nitrogen bearing species into a silicon dioxide layer overlying each of the wafers.

10. The method of claim 1 wherein the test wafer is a dummy wafer.

11. A method for processing integrated circuit memory devices, the method comprising:

preparing a plurality of test wafers identifiable by numbers from 1 through N, where N is an integer greater than 1, each of the test wafers including a predetermined thickness of dielectric material overlying the test wafer, the predetermined thickness of dielectric material being substantially a same thickness for each of the test wafers;

introducing a predetermined concentration of nitrogen bearing impurity from a plurality of different concentrations identifiable by numbers from 1 through N, where N is an integer greater than 1, into a respective test wafer identifiable by numbers 1 through N;

repeating the introducing for other test wafers until all test wafers numbered from 1 through N and all predetermined concentrations numbered from 1 through N are respectively introduced into test wafers numbered from 1 through N;

subjecting each of the test wafers to an oxidizing environment under selected conditions to cause growth to the dielectric layer on each of the test wafers, whereupon the growth is based for each test wafer based upon the predetermined concentration of nitrogen bearing impurity in the test wafer;

measuring a thickness of the dielectric material for each of the test wafers 1 through N, the thickness of the dielectric material for each of the test wafers being identifiable by numbers from 1 through N; and

correlating each of thickness numbered from 1 through N to each respective predetermined concentration numbered from 1 through N.

12. The method of claim 11 wherein the oxidizing environment is a rapid thermal oxidation process.

13. The method of claim 11 wherein N is at least 5.

14. The method of claim 11 wherein the correlation is a plot of thicknesses against concentrations.

15. The method of claim 11 wherein each of the test wafers is a silicon wafer of same characteristics.

16. A method for processing integrated circuit devices, the method comprising:

introducing a test wafer into a process for gate dielectric formation;

forming a silicon oxynitride layer to a predetermined thickness of less than 40 Angstroms at a predetermined temperature using a nitrogen bearing species on the test wafer;

forming a second oxidation overlying the silicon oxynitride layer to form an oxidation layer of a second thickness, the second thickness being based substantially upon a nitrogen bearing concentration of the nitrogen bearing species in the silicon oxynitride layer;

determining a parameter based upon at least the second thickness; and

using the parameter to determine a concentration of the nitrogen bearing species in the silicon oxynitride layer.

17. The method of claim 11 wherein the parameter is a thickness of the second thickness.

18. The method of claim 11 wherein the test wafer is included in a production run of wafers.

19. The method of claim 18 wherein the test wafer and the production run of wafers are provided into the process for gate dielectric formation.

20. The method of claim 19 wherein the test wafer is provided for an in-line test process, the in-line test process being substantially free from interference with the production run.